Moving Forward with OpenMP* Implementation in LLVM and Clang

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  ✓ Back-End: LLVM Prepass, Lowering and Outlining
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OpenMP* SIMD extension support in LLVM
  ✓ Declare SIMD support
  ✓ Vectorizing Loops with math function calls
Summary
What is OpenMP?

- De-facto standard Application Programming Interface (API) to write shared memory parallel applications in C, C++, and Fortran
- Consists of Compiler Directives, Runtime routines and Environment variables
- Specification maintained by the OpenMP Architecture Review Board (http://www.openmp.org)
- New ARB mission statement:
  - “The OpenMP ARB mission is to standardize directive-based multi-language high-level parallelism that is performant, productive and portable.”
- OpenMP* Specification Version 4.5 was launched in Now at SC’2015
OpenMP* Programming Model’s New Era

- CPUs and All forms of accelerators/coprocessors, GPU, APU, GPGPU, FPGA, and DSP
- Heterogenous consumer devices
  - Kitchen appliances, drones, signal processors, medical imaging, auto, telecom, automation, not just graphics engines – (Courtesy of Michael Wong (IBM) and Alexey Bataev (intel), et.al. LLVM Developer Conference Oct. 2105)
**OpenMP is widely supported by the industry, as well as the academic community**

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Programming Models Used at NERSC

- MPI dominates
- 40% of projects use OpenMP*

Courtesy of Yun (Helen) He, Alice Koniges, et. al., (NERSC) at OpenMPCon’2015
What is X if Use MPI+X at NERSC

✓ OpenMP is about 50%, out of all choices of X

Courtesy of Yun (Helen) He, Alice Koniges, et. al., (NERSC) at OpenMPCon’2015
Parallel + SIMD is the Path Forward

Intel® Xeon® and Intel® Xeon Phi™ Product Families are both going parallel

<table>
<thead>
<tr>
<th>Core(s)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>12</th>
<th>18</th>
<th>28</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threads</td>
<td>2</td>
<td>2</td>
<td>8</td>
<td>12</td>
<td>16</td>
<td>24</td>
<td>36</td>
<td>56</td>
</tr>
<tr>
<td>SIMD Width</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>256</td>
<td>256</td>
<td>256</td>
<td>512</td>
</tr>
</tbody>
</table>

More cores ➔ More Threads ➔ Wider vectors

OpenMP* is one of most important vehicles for the parallel + SIMD path forward

*Product specification for launched and shipped products available on ark.intel.com. 1. Not launched or in planning.
OpenMP* Programming Model

- Master thread spawns a team of threads / a league of thread teams as needed.
- Parallelism is added incrementally until desired performance is achieved: i.e. the sequential program evolves into a parallel program.
SAXPY: Coprocessor/Accelerator

```c
int main(int argc, const char* argv[]) {
    float *x = (float*) malloc(n * sizeof(float));
    float *y = (float*) malloc(n * sizeof(float));
    // Define scalars n, a, b & initialize x, y
    #pragma omp target data map(to:x[0:n])
    {
        #pragma omp target map(tofrom:y)
        #pragma omp teams num teams(num blocks) num_threads(bsize)
        all do the same
        #pragma omp distribute
        for (int i = 0; i < n; i += num blocks) {
            workshare (w/o barrier)
            #pragma omp parallel for
            for (int j = i; j < i + num blocks; j++) {
                workshare (w/ barrier)
                y[j] = a*x[j] + y[j];
            }
        }
        free(x); free(y); return 0;
    }
```
Data sharing / mapping: shared or distributed memory

Threads have access to a shared memory
- for shared data
- each thread can have a temporary view of the shared memory (e.g. registers, cache, etc.) between synchronization barriers.

Threads have private memory
- for private data
- Each thread has a stack for data local to each task it executes

- The corresponding variable in the device data environment may share storage with the original variable
- Writes to the corresponding variable may alter the value of the original variable
OpenMP* in Clang/LLVM: A Brief History

2H 2012: Several proposals with LLVM IR extensions and late outlining
✓ From Intel, Hal Finkel, others
✓ All of them involve changes to LLVM IR and thus, require modifications of LLVM phases
✓ None of them got enough support in the community

October 2012: OpenMP* in Clang project
✓ Started by AMD*, continued by Intel
✓ Early FE lowering and outlining
✓ OpenMP RTL calls generated in Clang

October 2015: OpenMP* 4.0 Target (Device) model supported in Clang FE
✓ Initial implementation available at https://github.com/clang-omp/clang_trunk
(Joint work by AMD, IBM, Intel and TI)

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10000ft View: High-Level Design for Moving Forward

Clang C/C++ FE

Par/Vec Prepass

ScalarOpts

LLVM IR Lowering and Outlining for OpenMP, Offload

Vectorization (explicit / auto)

Loop distribution

Loop fusion

Loop l'

Annotated par-loop for auto-parallelization

LLVM IR

LoopOpts

ScalarOpts

LLVM CG
LLVM OpenMP* Compiler Design Guideline

✓ Correctness: easy to achieve and maintain compiler intermediate states and consistency

✓ Competitive performance: compile-time and runtime performance

✓ Competitive code size: generated code size and adds-on module size from Intel implementation.

✓ Composite ability: analysis module and individual loop opts can composed flexibility to achieve high performance

✓ Debug ability: generate sufficient debug information

✓ Programmer friendly diagnostic and report messages
**LLVM IR Intrinsic Definitions**

def int_directive : Intrinsic<[], [llvm_metadata_ty],
                           [IntrReadWriteArgMem], "llvm.intel.directive">;

def int_directive_qual : Intrinsic<[], [llvm_metadata_ty],
                                     [IntrReadWriteArgMem], "llvm.intel.directive.qual">;

def int_directive_qual_opnd : Intrinsic<[], [llvm_metadata_ty, llvm_any_ty],
                                           [IntrReadWriteArgMem], "llvm.intel.directive.qual.opnd">;

def int_directive_qual_opndlist : Intrinsic<[], [llvm_metadata_ty, llvm_vararg_ty],
                                            [IntrReadWriteArgMem], "llvm.intel.directive.qual.opndlist">;

Each C++ obj is represented with four arguments: Value, default constructor, copy constructor and destructor.

* References to constructors / destructors are required to correctly create and destroy private copies of variables.

Array section is represented with (2 + # of DIMs x 3) arguments: Value, # of DIMs, lower0, length0, stride0, lower1, length1, stride1, ...
**LLVM IR Prepass**

✓ **CFG Restructuring**

✓ Transform parallel sections / worksharing sections to parallel loops / worksharing loops

✓ Pre-privatization renaming

✓ Multi-versioning for different targets (Host, GPU and Coprocessors)

✓ ... ...

```c
float parloop(float *a) {
    int k = 0;
    float x = 108.8f;
    //pragma omp parallel for simd reduction(+: x) shared(a) private(k)
    for (k=0; k<10000; k++) {
        x = x + a[k] + 100.08f;
    }
    return x;
}
```

```c
float x_temp = x;
@llvm.directive(DIR.OMP.PARALLEL.LOOP);
@llvm.directive.qual(DIR.QUAL.IS.OMP.SIMD);
@llvm.directive.qual.opnd.list(DIR.QUAL.REDUCTION.ADD,
    DIR.QUAL.OPND.VALUE,
    &x_temp);
@interface_qual_opnd_list(DIR_QUAL_SHARED,
    DIR_QUAL_OPND_VALUE, a, "opnd.end");
{ int priv_k;    //pragma omp parallel for simd reduction(+: x) shared(a)
    for (priv_k=0; priv_k<10000; priv_k++) {
        x_temp = x_temp + a[priv_k] + 100.08f;
    }
}  
@llvm.directive(DIR.OMP.END.PARALLEL.LOOP);
x = x_temp;
return x;
```
LLVM IR with Directive Intrinsics

`.str = private unnamed_addr constant [9 x i8] c"opnd.end\00", align 1
 ; Function Attrs: nounwind uwtable
define float @parloop(float* %a) #0 {
  entry:
    %x_temp = alloca float, align 4
    store float 0x405B333340000000, float* %x_temp, align 4, !tbaa
    call void @directive(i32 1) #2
    call void @directive.qual(i32 28) #2
    call void @directive.qual.opndlist(i32 3, i32 1, float* %x_temp, i8* getelementptr inbounds ([9 x i8]* @.str, i64 0, i64 0)) #2
    call void @directive.qual.opndlist(i32 1, i32 1, float* %a, i8* getelementptr inbounds ([9 x i8]* @.str, i64 0, i64 0)) #2
  %x_temp.promoted = load float* %x_temp, align 4, !tbaa
  br label %for.body
for.body:  ; preds = %for.body, %entry
  %indvars.iv = phi i64 [0, %entry], [ %indvars.iv.next, %for.body ]
  %add17 = phi float [ %x_temp.promoted, %entry ], [ %add1, %for.body ]
  %arrayidx = getelementptr inbounds float* %a, i64 %indvars.iv
  %0 = load float* %arrayidx, align 4, !tbaa
  %add = fadd float %add17, %0
  %add1 = fadd float %add
  %indvars.iv.next = add nuw nsw i64 %indvars.iv, 1
  %exitcond = icmp eq i64 %indvars.iv.next, 10000
  br i1 %exitcond, label %for.end, label %for.body
for.end:  ; preds = %for.body
  store float %add1, float* %x_temp, align 4, !tbaa
  call void @directive(i32 2) #2
  %1 = load float* %x_temp, align 4, !tbaa
  ret float %1
}`
LLVM CFG Restructuring
### LLVM IR Lowering and Outlining Passes

<table>
<thead>
<tr>
<th>Lowering</th>
<th>Outlining</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ Lowering</td>
<td>✓ Outlining</td>
</tr>
<tr>
<td>✓ Loop transformation (e.g. loop collapsing)</td>
<td>✓ Parallel regions/loops/sections/Tasks (use OpenMP runtime)</td>
</tr>
<tr>
<td>✓ Generate code for atomic, critical, single, master, ..., constructs (i.e. these constructs do not need outlining)</td>
<td>✓ Affinity setting</td>
</tr>
<tr>
<td>✓ Loop partitioning based on schedule type and chunk-size</td>
<td>✓ Generate runtime control code</td>
</tr>
<tr>
<td>✓ Generation code for reduction, lastprivate, firstprivate, copyprivate, ... threadprivate, etc.</td>
<td>✓ Target regions (use Offload runtime)</td>
</tr>
<tr>
<td>✓ Generate debug info and opt-reports</td>
<td>✓ Cilk for loops (use Cilk runtime)</td>
</tr>
<tr>
<td></td>
<td>✓ Packing / Unpacking arguments</td>
</tr>
<tr>
<td></td>
<td>✓ Generate debug info and opt-reports</td>
</tr>
</tbody>
</table>
Debugging Support

- Associate “privatized” LLVM VALUEs (variables) to original LLVM VALUEs (variables)
- Associate “argument” VALUEs of outlined function to original VALUEs
- LLVM debug info generation framework has similar functionalities for preserving debug info for privatization and data-sharing transformation.
typedef struct { float *x; float *a; } PARMLIST;

void __outlined_parloop(  
  int g_lower, int g_upper, int g_stride, PARMLIST *parms) {  
  int x_reduction; float *a; float *x;
  int t0 = 0, lower = 0, t1 = 0, upper = 0, stride = 1;
  int tid = __kmpc_global_get_thread_num();
  a = parms->a; x = parms->x;
  __kmpc_static_init(tid, &lower, &upper,
                     &stride, g_lower, g_upper, g_stride);
  x_red = 0.0f; t0 = lower; t1 = upper;
  @llvm.directive(DIR.OMP.SIMD);  
  @llvm.directive.qual.opndlist(DIR.QUAL.REDUCTION.ADD,
                                DIR.QUAL.OPND.VALUE, &x_red);
  for (int k=t0; k<t1; k++) {  
    x_red = x_red + a[k] + 100.8f;
  }  
  @llvm.directive(DIR.OMP.END.SIMD);  
  __kmpc_critical(tid);
  *x = *x + x_red;
  __kmpc_end_critical(tid);
  return;
}

float parloop(float *a) {  
  float  x = 108.8f;
  PARMLIST thunk;
  float x_temp = x;
  thunk.x = &x_temp;
  thunk.a = a;

  if (__kmpc_ok_fork()) {  
    __kmpc_fork_call(outlined_parloop, 0, 10000, 1, &thunk);
  } else {  
    __outlined_parloop(0, 10000, 1, &thunk);
  }
  x = x_temp;
  return x;
}
DECLARED SIMD: Function to Loop Conversion

Key Ideas:
- Produces correct scalar code for the function
- Treat function vectorization as loop vectorization

```
#pragma omp declare simd linear(i:1) uniform(x)
int foo(int i, int x) {
  return (x + i);
}
```

```
clang -c -emit-llvm -S -fopenmp-simd linear.c
```

```
attributes #0 = { nounwind uwtable "_ZGVxM4lu_" "_ZGVxN4lu_" ...
```
define __stdcall <4 x i32> @__ZGVbN4lu_foo(i32 %i, i32 %x) #0

entry:
%i.addr = alloca i32, align 4
%x.addr = alloca i32, align 4
store i32 %i, i32* %i.addr, align 4
store i32 %x, i32* %x.addr, align 4
%0 = load i32, i32* %x.addr, align 4
%1 = load i32, i32* %i.addr, align 4
%add = add nsw i32 %0, %1
ret i32 %add

return:
%cast = bitcast i32* %vec Cast to <4 x i32>*
%vec_ret = load <4 x i32>, <4 x i32>* %cast
ret <4 x i32> %vec_ret

simd.begin.region:
call void @llvm.directive(metadata !7)
call void @llvm.directive.qual.opnd.i32(metadata !8, i32 4)
call void (metadata, ...) @llvm.directive.qual.opndlist(metadata !9, i32 %i)
call void @llvm.directive.qual(metadata !10)

simd.loop:
%index = phi i32 [ 0, simd.begin.region ], [ %indvar, simd.loop.exit ]
store i32 %x, i32* %x.addr, align 4
%0 = load i32, i32* %x.addr, align 4
%1 = load i32, i32* %i.addr, align 4
%mul = mul i32 1, %index
%add.1 = add i32 %1, %mul
%add = add nsw i32 %0, %add.1
%vec_gep = getelementptr i32, i32* %vec Cast, i32 %index
store i32 %add, i32* %vec_gep

simd.loop.exit:
%indvar = add nsw i32 1, %index
%vlcond = icmp ult i32 %indvar, 4

simd.end.region:
call void @llvm.directive(metadata !11)
Vectorizing for Loop with Math Function Calls

icc sinf.c -fimf-max-error=0.6 -fimf-precision=high

#pragma omp simd
for (i = 0; i < 1000; i++) {
    array[i] = sinf(i);
}

Before Vectorization:

((F32) t0(F32)) = sinf(ic=SINF).imf_attrs(max-error=0.6 domain-exclusion=0 valid-status-bits=false precision=high)(
(F32) (EXPR_CONV.SI32.F32(i.219_V$3(SI32))(F32)); [CALL_CONVENTION_UNIX_ABI]

After Vectorization:

((MS128) t107(MS128)) = __svml_sinf4(ic=VX_VMLS_SIN4).imf_attrs(max-error=0.6 domain-exclusion=0 valid-status-bits=false precision=high)((MS128) t108(MS128)); [CALL_CONVENTION_UNIX_ABI]

Assembly:
..B1.2:                         # Preds ..B1.8 ..B1.7
    # Execution count [5.56e+00]
    cvtdq2ps %xmm8, %xmm0
    call __svml_sinf4_ha         #36.3
        # LOE rbx r12 r13 r14 r15 xmm0 xmm8 xmm9
Prototype Implementation

**Before Vectorization:**
%call = call float @sinf(float %div) #4, !dbg !22

Adding a Clang FE patch would be something like:
%call = call float @llvm.sin.f32(float %div) #4, !dbg !22

**After Vectorization:**
%4 = call <4 x float> @llvm.sin.v4f32(<4 x float> %3), !dbg !27, !imf-precision !10, !imf-max-error !11

!10 = !{"imf-precision=high"}
!11 = !{"imf-max-error=0.6"}

**After SVML translation pass:**
%3 = call <4 x float> @_svml_sinf4_ha(<4 x float> %2)
Prototype Implementation with XMM

vector.body: ; preds = %vector.body, %entry
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ], !dbg !2
%0 = trunc i64 %index to i32, !dbg !7
%broadcast.splatinsert6 = inseretelement <8 x i32> undef, i32 %0, i32 0, !dbg !7
%broadcast.splat7 = shufflevector <8 x i32> %broadcast.splatinsert6, <8 x i32> undef, <8 x i32> zeroinitlizer, !dbg !7
%induction8 = add <8 x i32> %broadcast.splat7, <i32 0, i32 1, i32 2, i32 3, i32 4, i32 5, i32 6, i32 7>, !dbg !7
%1 = sitofp <8 x i32> %induction8 to <8 x float>, !dbg !7
%shuffle = shufflevector <8 x float> %1, <8 x float> undef, <4 x i32> <i32 0, i32 1, i32 2, i32 3>
%vcall = call <4 x float> @__svml_sinf4_ha(<4 x float> %shuffle)
%shuffle.1 = shufflevector <8 x float> %1, <8 x float> undef, <4 x i32> <i32 4, i32 5, i32 6, i32 7>
%vcall.2 = call <4 x float> @__svml_sinf4_ha(<4 x float> %shuffle.1)
%shufflecomb = shufflevector <4 x float> %vcall, <4 x float> %vcall.2, <8 x i32> <i32 0, i32 1, i32 2, i32 3, i32 4, i32 5, i32 6, i32 7>
%2 = getelementptr inbounds float, float* %array, i64 %index, !dbg !8
%3 = bitcast float* %2 to <8 x float>* , !dbg !9
store <8 x float> %shufflecomb, <8 x float>* %3, align 4, !dbg !9, !tbaa !10
%index.next = add i64 %index, 8, !dbg !2
%4 = icmp eq i64 %index.next, 1000, !dbg !2
br i1 %4, label %for.end, label %vector.body, !dbg !2, !llvm.loop !14

#pragma omp simd simdlen(8)
for ( i = 0; i < 1000; i++) {
    array[i] = sinf(i);
}
Summary

✓ OpenMP is evolving with a set of new features that needs scalar optimization, vectorization and loop optimizations to be seamlessly integrated with parallelization (privatization, lowering, outlining, ... etc.)
✓ Multiple languages support with effective engineering and maintaining cost
✓ Path-finding efforts to study feasibility of the Back-End solution
  ✓ Minimal extensions for LLVM IR
  ✓ Minimal Impact on LLVM infrastructure and optimizations
  ✓ Getting optimal threaded code to leverage target HW potential
  ✓ Targeting modern CPUs, Coprocessors, GPUs, DSP, FPGA, ... etc.
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